DEC STD 176-6 Single-Sided/Double-Sided Nonplated Through (SS/DS) Printed-Wiring Board Acceptance Criteria

DOCUMENT IDENTIFIER: A-DS-EL00176-06-0000 Rev B, 11-Nov-1992

ABSTRACT: This manufacturing standard specifies end-product criteria for rigid printed-wiring boards (PWBs) that have been fabricated by or purchased for Digital Equipment Corporation.

NOTE

This standard must be used with *DEC STD 176-0 Printed-Wiring Board Acceptance Criteria*.

APPLICABILITY: Whether fabricated in Digital manufacturing facilities or purchased from qualified suppliers, all printed-wiring boards (PWBs) shall meet or exceed all applicable specifications found in this standard, as modified only by related Digital drawings and specifications.

STATUS: APPROVED 11-Nov-1992; use VTX SMC for current status.

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CONTENTS

1 INTRODUCTION 1
1.1 SCOPE 1
1.2 RESPONSIBILITIES 1
1.2.1 Digital Organizations 1
1.2.2 Suppliers 1
1.2.3 PWB Standards Committee 2

2 GENERAL REQUIREMENTS 2
2.1 TERMINOLOGY 2
2.2 COMPOSITION AND PROCESSING 2
2.3 OVERALL CONFIGURATION AND CONSTRUCTION 2
2.4 MICROSECTIONING AND MAGNIFICATION 2
2.5 ROUNDING CONVENTION 2
2.6 FABRICATION MATERIALS 3
2.7 WORKMANSHIP AND CLEANLINESS 3
2.8 IDENTIFICATION MARKINGS 3
2.9 COLORS 3
2.10 DIMENSIONS AND TOLERANCES 3

3 OUTSIDE CONFIGURATION 3
3.1 WARPAGE 3
3.2 SLOTS, NOTCHES, AND CUTOUTS 4
3.3 STRAIGHTNESS, PARALLELISM, AND SQUARENESS 4

4 BASE MATERIAL VISUAL CHARACTERISTICS 4

5 HOLES 4
5.1 NONPLATED DRILLED AND PUNCHED HOLES 4
5.1.1 Nonplated Hole Diameters 4
5.1.2 Chips, Cracks, Delamination, Fibers, Haloing—Drilled and Punched Holes 4
5.1.3 Missing and Extra Holes 4
5.2 HOLE LOCATION ACCURACY (HLA) 5

6 CONDUCTORS AND PADS 6
6.1 CONDUCTOR WIDTHS 6
6.2 SPACING 6
6.3 PAD DIAMETERS 7
6.4 ANNULAR RINGS—MAXIMUM ALLOWABLE MISREGISTRATION FOR SINGLE-SIDED, DOUBLE-SIDED, NONPLATED THROUGH TECHNOLOGIES . 7
6.4.1 Outer-Layer Features 7
6.5 PLATING THICKNESSES—ETCH LINES (SINGLE-SIDED, DOUBLE-SIDED, NONPLATED THROUGH) 8

7 PLATING CHARACTERISTICS 10
7.1 TIN-LEAD PLATING (FUSED) 10
7.2 ADHESION 10
7.3 BOND STRENGTH (TERMINAL PULL STRENGTH) 10

7.4 SOLDERABILITY 10
8 FINGERS 10
9 SOLDERMASK 10
9.1 TYPES 11
9.2 PLACEMENT 11
9.2.1 Board Side 11
9.2.2 Spacing/Coverage Requirements for Single-Sided, Double-Sided, Nonplated Through 11
10 MULTILAYER (ML) AND MULTISIGNAL-LAYER (MSL) PWBs 11
11 AUTOTHIEVING AND OTHER NONCONDUCTOR ETCH 11
11.1 NONCONDUCTOR ETCH 11
12 BACKPANEL BOARDS 11
13 ELECTRICAL CHARACTERISTICS 11
13.1 CONDUCTOR INTERCONNECTION RESISTANCE 12
13.2 CONTINUITY 12
14 ALLOWABLE REPAIRS 12
15 PRODUCT SAFETY 12
16 NONCONFORMING BOARDS 12
17 PACKAGING 12
18 QUALITY ASSURANCE TESTS 12

Appendix A REFERENCED DOCUMENTS 13
A.1 Digital Documents, EL-Class 13
A.2 Digital Documents, Other Than EL-Class 13
A.3 Documents External to Digital 13
A.4 Ordering Information 13

FIGURES

1 Preferred Hole-to-Pad Registration 7
2 Maximum Hole-to-Pad Breakout 8
3 Minimum Annular Ring—No Elongated Pad 8
4 Plating Thickness—Etch Lines 9

TABLES

1	Printed-Wiring Board Configurations	1
2	Magnification	2
3	Maximum Warpage	3
4	Nonplated Hole Diameters	4
5	Conductor Widths (Singe-Sided, Double-Sided, Nonplated Through)	6
6	Spacing (Single-Sided, Double-Sided, Nonplated Through)	6
7	Pad Diameters	7
8	Plating Thickness—Etch Lines	9

1 INTRODUCTION

This manufacturing document specifies end product criteria for rigid single-sided/double-sided nonplated-through hole printed-wiring boards (PWBs) that have been fabricated or purchased by Digital Equipment Corporation.

1.1 SCOPE

This standard specifies the final end product acceptance criteria for single-sided, double-sided (SS/DS) nonplated through rigid PWBs of the types and technology codes specified in *DEC STD 176-0 Printed-Wiring Board Acceptance Criteria*, Table 1. This standard is intended to augment information presented in DEC STD 176-0 where final end product criteria for SS/DS nonplated through PWBs differs from conventional plated tin-lead/reflowed printed-wiring boards. This standard does not apply to flex circuits or ceramic printed-wiring substrates.

Table 1: Printed-Wiring Board Configurations

Standard Plane Technology	Layer Description and Order		
		Single-Sided No PTH	Double-Sided No PTH
	GDC Code Block 1	Layer GDC Code Block 2 A	Layer GDC Code Block 2 B
25/25	A	AA	AB
20/20	B	BA	BB
15/15	C	CA	CB
12/13	D	DA	DB

1.2 RESPONSIBILITIES

This section describes specific responsibilities of persons or organizations for fulfilling the requirements of this standard.

1.2.1 Digital Organizations

All internal organizations involved in the fabrication, procurement, and use of PWBs are responsible for understanding and complying to the requirements in this document and for providing information to keep the document up to date.

1.2.2 Suppliers

Suppliers under contract to produce PWBs for Digital must comply with the requirements of this standard.

1.2.3 PWB Standards Committee

Refer to EL-SM176-00 *Printed-Wiring Board Manual*, for a list of committee members.

2 GENERAL REQUIREMENTS

All PWBs shall meet or exceed all applicable specifications found in this standard, as modified only by related Digital drawings and specifications.

2.1 TERMINOLOGY

The definitions of all printed-wiring terms used in this standard shall be as specified in *DEC STD 016-0 Printed-Wiring Board and Module Manufacturing Terminology.*

2.2 COMPOSITION AND PROCESSING

The composition and processing of the types of PWBs covered by this standard shall be as described in DEC STD 016-0.

2.3 OVERALL CONFIGURATION AND CONSTRUCTION

Refer to DEC STD 176-0, subhead 2.3.

2.4 MICROSECTIONING AND MAGNIFICATION

Microsection inspections shall be in accordance with text under subhead 2.1.1 of IPC-TM-650, *Test Methods Manual*.

The appropriate magnification for defect detection is specified in Table 2. When a defect is suspected at these magnifications, higher magnification may be used to verify conformance and assist in determining the root cause. Defects found at higher magnification are considered defects.

Table 2: Magnification

Item(s) Inspected	Minimum Magnification (X)
Overall cosmetic quality	Visual inspection
Board features	2
Referee inspection of board features	10
Plating quality in microsections	200
Plating and soldermask thickness in microsections	400

2.5 ROUNDING CONVENTION

See DEC STD 176-0, subhead 2.5.

2.6 FABRICATION MATERIALS

See DEC STD 176-0, subhead 2.6.

2.7 WORKMANSHIP AND CLEANLINESS

See DEC STD 176-0, subhead 2.7.

2.8 IDENTIFICATION MARKINGS

See DEC STD 176-0, subhead 2.8.

2.9 COLORS

See DEC STD 176-0, subhead 2.9.

2.10 DIMENSIONS AND TOLERANCES

See DEC STD 176-0, subhead 2.10.

3 OUTSIDE CONFIGURATION

See DEC STD 176-0, head 3.

3.1 WARPAGE

When measured in accordance with DEC STD 176-0, Appendix C, the maximum warpage (bow or twist) shall be as listed in Table 3.

Table 3: Maximum Warpage

Nominal Board Thickness		Maximum Warpage Ratio
inch	mm	
Single-Sided/Double-Sided Nonplated Through		inch/inch
Less than 0.063	Less than 1.6	0.015
0.063 through 0.094	1.6 through 2.38	0.010
Over 0.094 through 0.125	Over 2.38 through 3.18	0.008
Over 0.125	Over 3.180	0.006
Single-Sided/Double-Sided, Nonplated Through with SMT and Mixed-Mount Components		
Less than 0.094	Less than 2.38	0.007
Over 0.094 through 0.250	Over 2.38 through 6.35	0.005

3.2 SLOTS, NOTCHES, AND CUTOUTS

See DEC STD 176-0, subhead 3.5.

3.3 STRAIGHTNESS, PARALLELISM, AND SQUARENESS

See DEC STD 176-0, subhead 3.6.

4 BASE MATERIAL VISUAL CHARACTERISTICS

See DEC STD 176-0, head 4.

5 HOLES

The criteria for nonplated holes are as follows.

5.1 NONPLATED DRILLED AND PUNCHED HOLES

Requirements are specified in the following paragraphs for nonplated hole diameters, pattern accuracy, chips, cracks, fibers, haloing, delamination, and missing and extra holes.

5.1.1 Nonplated Hole Diameters

Unless otherwise specified, drilled, punched, or routed hole diameter tolerances shall be as listed in Table 4 and shall not contain any plating. The preferred method of measurement is using pin gauges.

Table 4: Nonplated Hole Diameters

Nominal Diameters		Tolerances	
inches	mm	inches	mm
Under 0.125	Under 3.20	±0.004	±0.10
0.125 to 0.250	3.20 to 6.35	±0.005	±0.3
0.251 and over	6.38 and over	± 0.020	±0.51

NOTE

Nominal tooling hole diameter and tolerances are 0.250 inch, +0.000 inch/-0.003 inch (6.35 mm, +0.000 mm/-0.076 mm); 0.157 inch, ±0.003 inch (4.00 mm, ±0.076 mm).

5.1.2 Chips, Cracks, Delamination, Fibers, Haloing—Drilled and Punched Holes

See DEC STD 176-0, subhead 5.1.2.

5.1.3 Missing and Extra Holes

See DEC STD 176-0, subhead 5.1.3.

5.2 HOLE LOCATION ACCURACY (HLA)

See DEC STD 176-0, subhead 5.2.

Hole Location Accuracy (HLA) shall be determined with a properly calibrated, coordinate measuring machine with suitable accuracy, precision, and repeatability. All measurements shall be performed on finished product from Side 1. For a multiple circuit board, HLA shall be assessed on an individual circuit basis. HLA shall be measured from an absolute reference datum (typically a dimensioned hole) to a hole including assembly rezero holes. The assembly rezero holes are used by Digital Module Assembly as zero reference locations for autoinsertion. The rezero holes are identified on the assembly board drawing and shall meet the following requirements.

a. Drilled during the same *setup* as the drilling of conductive pattern holes.

b. Typically the same diameter as the predominant drilled hole size. However, diameters should not exceed the range 0.035 inch (0.90 mm) minimum to 0.047 inch (1.20 mm) maximum.

c. The surface edges and inner diameter shall be clear of all foreign material and shall not be damaged or distorted in any way.

The HLA for holes that are drilled shall be:

Geometric location tolerance (GLT): ±0.003 inch (0.076 mm)
True position diameter (TPD): 0.0085 inch (0.216 mm)

The HLA for holes that are *punched* shall be 0.014 inch (0.356 mm) TPD, ± 0.005 inch (± 0.127 mm) GLT. Use the same procedure for determining hole location accuracy as described for drilled holes.

Refer to DEC STD 176-0 Appendix B for calculation of TPD/GLT.

6 CONDUCTORS AND PADS

Conductor widths and spacing, pad diameters, annular rings, plating thicknesses, edge characteristics, and other characteristics are specified in the following sections.

6.1 CONDUCTOR WIDTHS

Unless otherwise specified, when measuring for edge definition in accordance with subhead 2.2.3 of IPC-TM-650, the minimum conductor widths measured at the base laminate—foil (plating) interface shall be in accordance with Table 5.

Table 5: Conductor Widths (Singe-Sided, Double-Sided, Nonplated Through)

Technology Code	Nominal Width*		Minimum Width**		Density Level
	inches	mm	inches	mm	
B	0.020	0.51	0.015	0.38	Standard
C	0.015	0.38	0.011	0.28	High
D	0.012	0.30	0.008	0.20	High

* Design nominal for reference only.
** The minimum for all nonstandard conductor widths greater than 0.020 inch (0.51 mm) shall be the nominal minus 0.005 inch (0.13 mm).

6.2 SPACING

Minimum conductor-to-conductor, conductor-to-pad, and pad-to-pad spacing for all layers shall be in accordance with Table 6.

Table 6: Spacing (Single-Sided, Double-Sided, Nonplated Through)

Technology Code	Conductor To	Nominal Spacing*		Minimum Spacing**		Nominal* Pad Size
		inches	mm	inches	mm	
B (20/20)	Conductor	0.020	0.51	0.015	0.38	0.080 x
	Pad	0.020	0.51	0.015	0.38	0.100
C (15/15)	Conductor	0.018	0.46	0.009	0.23	0.080 x
	Pad	0.015	0.38	0.009	0.23	0.100
D (12/13)	Conductor	0.013	0.33	0.009	0.23	0.080 x
	Pad	0.017	0.43	0.009	0.23	0.100

* Design nominal for reference only.
** The minimum for all nonstandard spacing greater than 0.020 inch (0.51 mm) shall be the nominal minus 0.005 inch (0.13 mm).

6.3 PAD DIAMETERS

Minimum pad diameters shall be in accordance with Table 7.

Table 7: Pad Diameters

Technology Code	Nominal Diameter*		Minimum Diameter**		Density Level
	inches	mm	inches	mm	
B, C, D	0.080 x 0.100	2.03 x 2.54	0.075 x 0.095	1.90 x 2.41	Standard /High

* Design nominal for reference only.
** Unless specified otherwise, the minimum diameter for special assembly pads shall be nominal diameter minus 0.003 inch (0.076 mm).

NOTE

The minimum for all other pad diameters shall be the nominal diameter minus 0.005 inch (0.13 mm).

6.4 ANNULAR RINGS—MAXIMUM ALLOWABLE MISREGISTRATION FOR SINGLE-SIDED, DOUBLE-SIDED, NONPLATED THROUGH TECHNOLOGIES

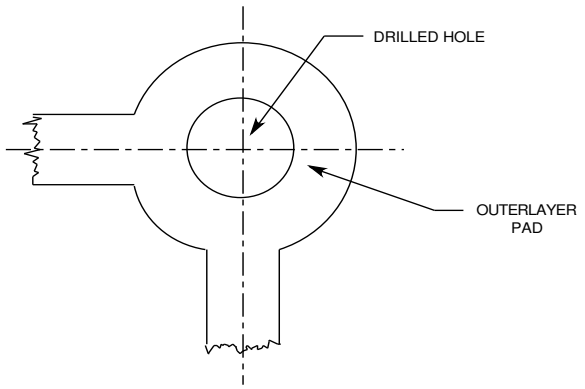
The following conditions are the maximum allowable for both MSL and Non-MSL technologies.

6.4.1 Outer-Layer Features

Acceptability levels for outer-layer annular rings for all holes are specified as follows. Hole location should meet the criteria in DEC STD 176-0, subhead 6.4.1.

a. **Preferred**

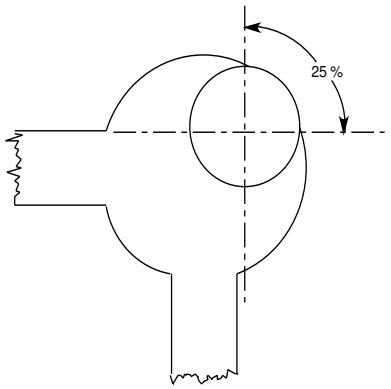
Figure 1: Preferred Hole-to-Pad Registration



Hole concentric with the pad.

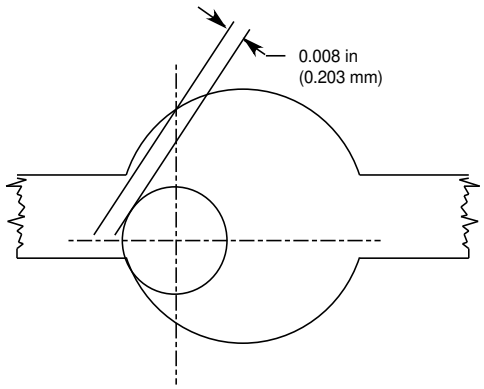
b. **Maximum Acceptable Breakout—Outer Layer Features**

Figure 2: Maximum Hole-to-Pad Breakout



Hole intersecting pad edge with 25 percent hole breakout.

Figure 3: Minimum Annular Ring—No Elongated Pad



Hole tangent to pad edge at one side of conductor-pad interface with 0.008 inch (0.2032 mm) between hole and other side of interface.

6.5 PLATING THICKNESSES—ETCH LINES (SINGLE-SIDED, DOUBLE-SIDED, NONPLATED THROUGH)

As determined via microsectioning and appropriate magnification, DEC STD 176-0, subhead 2.4, the minimum conductor plating thicknesses at the crest shall be as specified in Figure 4, unless specified otherwise.

Figure 4: Plating Thickness—Etch Lines

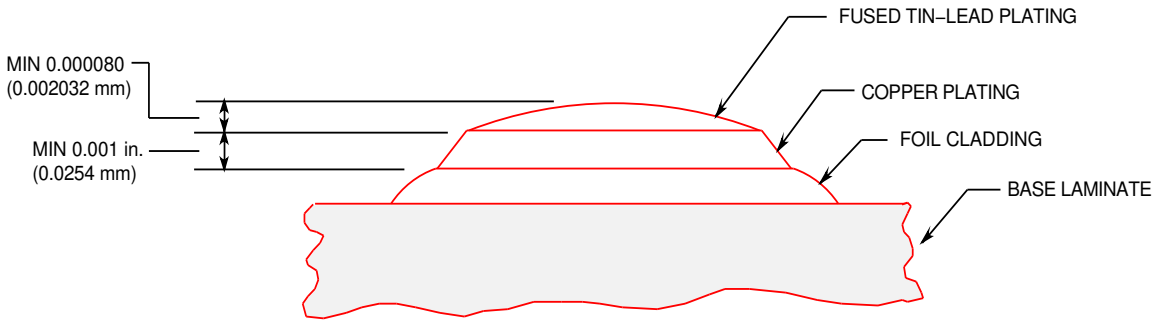


Table 8: Plating Thickness—Etch Lines

Plating Material	Minimum Thickness
Electroless copper	Sufficient for subsequent copper electroplating.
Electrolytic copper	0.001 inch (0.03 mm).
Fused tin-lead and solder	0.000080 inch (0.00203 mm) crest. Total coverage on conductor/pad side wall preferred but not required.

NOTE

All Copper boards are acceptable if solderability meets Digital requirements. See *DEC STD 176-5 Printed-Wiring Board Acceptance Criteria for All Copper Product*.

7 PLATING CHARACTERISTICS

The following describes the required criteria related to Plating characteristics.

7.1 TIN-LEAD PLATING (FUSED)

Fusing of tin-lead plating is required on all solderable surfaces. All nonterminal areas of conductors and power/ground planes may be dewetted. All tin-lead plated surfaces shall be 50-70 percent tin (30-50 percent lead) content. The fused tin-lead shall be 0.00008 inch (0.00203 mm) thick minimum when measured at the crest. Total coverage of conductor/pad sidewall preferred but not required.

7.2 ADHESION

See DEC STD 176-0, subhead 7.2.

7.3 BOND STRENGTH (TERMINAL PULL STRENGTH)

This subhead is not applicable to single-sided, double-sided, nonplated through.

7.4 SOLDERABILITY

Holes and terminal areas that will be soldered shall demonstrate at least 95 percent wetting with 5 percent unconcentrated dewetting and pinholing allowed; there shall be no evidence of nonwetting. All nonterminal areas of power and ground planes may be unfused and may be dewetted. Refer to IPC-S-804, *Solderability Test Methods for Printed Wiring Boards.*

Solderability tests shall be in accordance with IPC-S-804. Regardless of the test method used, the following shall occur.

a. Proper wetting of the surface and terminal area

b. No blistering, delamination (lifted conductors) or other forms of degradation of the conductive pattern

8 FINGERS

See DEC STD 176-0, subhead 8.

9 SOLDERMASK

Soldermask shall cover etches to prevent bridging during the module solder process.

Soldermask types, placement, thickness, cure, solvent/flux resistance, flammability, abrasion resistance, adhesion, soldering requirements, and other characteristics are specified in the following sections. These requirements apply for solder side when a mask is applied.

9.1 TYPES

When required, a full soldermask as described in DEC STD 176-0 will be on the solder side of all PWBs as specified in the following.

9.2 PLACEMENT

Soldermask placement and spacing requirements are specified in the following subheads.

9.2.1 Board Side

The following placements and masks are allowed.

a. All high density boards (C) with nominal conductor widths and spacings of 0.015 inch (0.38 mm) must have full soldermask on the solder side.

b. All high density boards (D) with nominal conductor widths of 0.012 inch (0.31 mm) and nominal conductor spacing of 0.013 inch (0.33 mm) must have a full soldermask on the solder side as a minimum.

c. Unless otherwise specified, standard density boards (A,B) with conductor widths and spacings of 0.020 inch (0.51 mm) do not require soldermask.

9.2.2 Spacing/Coverage Requirements for Single-Sided, Double-Sided, Nonplated Through

Soldermask spacing requirements are as follows.

a. The soldermask shall extend over both sides of the conductor or pad to the base laminate.

b. On all single-sided, double-sided, nonplated through PWBs, the soldermask shall not be closer than 0.008 in (0.203 mm) to component holes.

10 MULTILAYER (ML) AND MULTISIGNAL-LAYER (MSL) PWBs

This subhead does not apply to single-sided, double-sided, nonplated through.

11 AUTOTHIEVING AND OTHER NONCONDUCTOR ETCH

See DEC STD 176-0, head 11, if required.

11.1 NONCONDUCTOR ETCH

See DEC STD 176-0, subhead 11.2.

12 BACKPANEL BOARDS

This heading does not apply to single-sided, double-sided, nonplated through.

13 ELECTRICAL CHARACTERISTICS

Interconnection resistance and continuity are specified in the following.

13.1 CONDUCTOR INTERCONNECTION RESISTANCE

When measured in accordance with IPC-TM-650, the interconnection resistance from any terminal area (pad or finger) to any other terminal area on the same side of the board shall not be greater than 0.001 ohm for each 0.125 inch (3.18 mm) of conductor length.

NOTE

This subhead requires use of the IPC-TM-650 test pattern.

13.2 CONTINUITY

There shall be no shorts between adjacent conductor, or between adjacent networks of interconnected conductors, as defined in the design data base. There shall be no opens between any conductors or networks defined as connected in the design data base.

14 ALLOWABLE REPAIRS

Digital and non-Digital Equipment Corporation supplier personnel may perform repairs as specified in *DEC STD 176-1 Printed-Wiring Board Repair Criteria.* After repair, the board must meet all physical, electrical, cosmetic, workmanship, and cleanliness requirements specified in this standard.

15 PRODUCT SAFETY

All Product Safety and UL requirements are specified in *DEC STD 176-2 Printed-Wiring Board Product Safety Criteria*.

16 NONCONFORMING BOARDS

All nonconforming PWBs shall be processed in accordance with Digital engineering specification A-SP-7665075-00-0, *Procedure for Processing Nonconforming Material and In-Process Waiver.*

17 PACKAGING

See DEC STD 176-0, subhead 16.

18 QUALITY ASSURANCE TESTS

See DEC STD 176-0, subhead 17.

APPENDIX A REFERENCED DOCUMENTS

A.1 Digital Documents, EL-Class

Document Number	Document Title
EL-00016-00	*DEC STD 016-0 Printed-Wiring Board and Module Manufacturing Terminology*
EL-00176-00	*DEC STD 176-0 Printed-Wiring Board Acceptance Criteria*
EL-00176-01	*DEC STD 176-1 Printed-Wiring Board Repair Criteria*
EL-00176-02	*DEC STD 176-2 Printed-Wiring Board Product Safety Criteria*
EL-00176-05	*DEC STD 176-5 Printed-Wiring Board Acceptance Criteria for All Copper Product*
EL-SM176-00	*Printed-Wiring Board Manual*

A.2 Digital Documents, Other Than EL-Class

Document Number	Document Title
A-SP-7665075-00-0	*Procedure for Processing Nonconforming Material and In-Process Waiver*

A.3 Documents External to Digital

Document Number	Document Title
IPC-S-804	*Solderability Test Methods for Printed-Wiring Boards*
IPC-TM-650	*Test Methods Manual*

A.4 Ordering Information

Use VTX SMC to order copies of EL-class documents from Standards and Methods Control. Send distribution questions to JOKUR::SMC or call DTN: 234-4423.

Following are the sources for documents not available from Standards and Methods Control.

- Institute for Interconnecting and Packaging Electronic Circuits

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